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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,347	04/27/2001	Jun Zeng	SE1645PD (50042)	2463

7590 06/18/2003

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EXAMINER	
SOWARD, IDA M	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,347	ZENG, JUN	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Applicant's amendment filed March 31, 2003.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 23-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Admitted Prior Art Figures 1 and 3a-3b.

Prior Art Figures 1 and 3a-3b teach a semiconductor layer **9** having a trench **14** therein; a gate dielectric layer **24** lining the trench; a gate conducting layer **12** in a lower potion of the trench; a dielectric layer **20** in an upper portion of the trench and extending outwardly from the semiconductor layer; source regions **26** adjacent the outwardly extending dielectric layer; source/body contact regions **18** laterally spaced from the gate conducting layer and non-interruptibly contacting the source regions; and a source electrode **22** on the source regions and on the dielectric layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25, 27, 32 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figures 1 and 3a-3b as applied to claims 23-24 above, and further in view of Gilbert et al. (5,349,224).

Prior Art Figures 1 and 3a-3b teach all mentioned in the rejection above. Prior Art Figures 1 and 3a-3b further teach a source electrode **22** on the source regions **26**, on the dielectric layer **20**, and on the source/body contact regions **18**; a gate dielectric layer **24** lining the trench. However, Prior Art Figures 1 and 3a-3b fail to teach at least one conductive via between the source electrode and the source/body contact region. Gilbert et al. teach at least one conductive via between the source electrode **90** and the source/body contact region **64** (Figure 5F). Gilbert et al. further teach the source electrode on the source region, on the dielectric layer and on the conductive via; and an opening exposing the source/body contact region, wherein the source/body contact regions are exposed by an opening in the source region (Figure 5F). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the MOSFET of Prior Art Figures 1 and 3a-3b and with the MOSFET having conductive vias of Gilbert et al. to be readily integrable in a semiconductor integrated circuit (col. 1, lines 6-11).

Claims 26, 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figures 1 and 3a-3b and Gilbert et al. (5,349,224) as applied to claims 23-24 above, and further in view of Grabowski et al. (6,140,678).

Prior Art Figures 1 and 3a-3b and Gilbert et al. teach all mentioned in the rejections above. However, Prior Art Figures 1 and 3a-3b and Gilbert et al. fail to teach a recess over the source/body contact regions wherein the source/body contact regions are recessed within the semiconductor layer adjacent the source regions. Grabowski et al. teach a recess over the source/body contact regions **33** wherein the source/body contact regions are recessed within the semiconductor layer **14** adjacent the source regions **34** (Figure 4A). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the MOSFET of Prior Art Figures 1 and 3a-3b and MOSFET having conductive vias of Gilbert et al. with the MOSFET having recessed areas of Grabowski et al. to reduce hot carrier injection (col. 1, lines 46-65).

Claim 29, 31, 35 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figures 1 and 3a-3b and Gilbert et al. (5,349,224) as applied to claim 23-24 above, and further in view of Shih et al. (5,283,452).

Prior Art Figures 1 and 3a-3b and Gilbert et al. teach all mentioned in the rejections above. However, Prior Art Figures 1 and 3a-3b and Gilbert et al. fail to teach a gate recess depth within a range of 0.2 to 0.8 microns. Shih et al. teach a gate recess depth of 0.25 microns (col. 5, lines 67-68). In regard to claim 31, since Shih et al. teach

an optimal gate recess depth of 0.25 microns, it is within the art of ordinary skill to provide an upper surface of the recess of less than 1 micron. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the MOSFET of Prior Art Figures 1 and 3a-3b and the MOSFET having conductive vias of Gilbert et al. with the FET having the gate recess depth of Shih et al. to achieve high power operation (col. 61-68).

Claims 28, 34 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figures 1 and 3a-3b and Gilbert et al. (5,349,224) as applied to claim 23-24 above, and further in view of Singh et al. (5,960,311).

Prior Art Figures 1 and 3a-3b and Gilbert et al. teach all mentioned in the rejections above. However, Prior Art Figures 1 and 3a-3b and Gilbert et al. fail to teach a dielectric layer extending from a region equal to or less than about 1 micron. Singh et al. teach a dielectric layer extending from a region from 0.5 to 1.2 microns (col. 5, lines 21-26). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the MOSFET of Prior Art Figures 1 and 3a-3b and the MOSFET having conductive vias of Gilbert et al. with the MOSFET having a dielectric layer extending from a region of Singh et al. to increase the speed of integrated circuits (col. 3, lines 33-36).

Response to Arguments

Applicant's arguments filed 03-31-03 have been fully considered but they are not persuasive.

Admitted Prior Art Figures 3a-3b disclose a dielectric layer 20 in an upper portion of the trench 14 and extending outwardly from the semiconductor layer 16, the outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-

3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 7:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-308-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
June 12, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800